It is desirable to achieve multi-bit performances using the sum of single bit modulators, which inherently have better stability and performance. A multi-bit modulator is designed for high-resolution systems. The DEM block adds latency, area, and power consumption, so the modulator has been simulated with MATLAB Simulink to assess its performance. It is possible to trade off amplitude resolution for time resolution, which is more expensive in modern integrated circuits, using the Delta-Sigma (∆Σ) modulation technique: the quantization noise is pushed out of band thanks to a combination of input signal oversampling and the DEM modulation scheme.

Nowadays it is easy to automate digital circuit designs and make them future-proof thanks to the Moore law of exponentially increasing digital computation power. Analog design is more difficult to address, requiring tight tolerances (expensive calibrations and trimming in high-end integrated circuits) and high power consumptions to overcome mismatch and noise-related errors. This increases the cost and the reliability of the final device.

High performance DACs can be used as a building block for high quality Analog-to-Digital Converters (ADCs), assuming that the DAC ensures a good linearity.

High performance DACs and ADCs are often needed in real-life applications, leading to mixed-signal integrated circuits which are difficult to design. Hence the need of remaining "as most digital as possible" to be less affected by the analog errors.

It is possible to trade off amplitude resolution for time resolution, much cheaper in modern integrated circuits, using the Delta-Sigma (∆Σ) modulation technique: the quantization noise is pushed out of band thanks to a combination of input signal oversampling and quantization noise shaping.

1 bit DACs (featuring just two possible levels) are inherently linear while multi-bit (∆Σ) DACs are prone to analog errors, in particular static mismatches that generate nonlinear distortions. In return, multi-bit DACs are less sensitive to dynamic errors like clock jitter and inter-symbol interference (ISI).

A linear multi-level DAC is usually achieved with a multi-bit ∆Σ modulator and a Dynamic Element Matching (DEM) scheme. The DEM maps the multi-bit digital word to a finite set of single bit DACs in a thermometer-like fashion but following some constraints in order to tame the mismatch (by ensuring equal utilization of all the single DAC elements) and, in recent works, the ISI by means of complicated digital schemes (by ensuring a more or less constant transition density value for each DAC element).

The DEM block adds latency, area and power consumption: the DEM, in fact, decomposes the multi-bit signal as a sum of single bits, following a local ∆Σ scheme. The complexity of the DEM grows exponentially with respect to the number of bits required and it is difficult to make high order DEMs.

It is difficult to design stable single bit ∆Σ modulators with high in-band Signal-to-Quantization Noise Ratio (SQNR). A multi-bit modulator is inherently much more stable and achieves higher SQNR values but it is difficult to replicate the outcome of the digital modulator in the analog domain as each nonlinearity (in particular harmonic distortion) adds up as noise, degrading the Signal to Noise Ratio (SNR).

It is desirable to achieve multi-bit performances using the sum of single bit modulators, hence guaranteeing linearity, low out-of-band noise, high SNR, low latency, insensitivity to analog errors (both static and dynamic ones), high order ∆Σ modulator stability.

Research context and motivation

• Many smart signal processing tasks can be carried out in the digital domain thanks to the robustness and reliability of numeric computation but the physical world needs to deal with analog signals, thus the need for high quality Digital-to-Analog Converters (DACs).

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Addressed research questions/problems

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Novel contributions

• A new topology for multi-level ∆Σ is here presented. It features nested feedback loops for handling at the same time both the single bit modulation and the multi-bit part. Each output DAC element carries the whole input signal plus the shaped quantization noise component. The global feedback loop minimizes the sum of the total in-band noise, acting as a multi-bit modulator, while the inner loop is dedicated to the noise shaping of the local modulator. The chain of delays in the output of the local modulator is employed to shift in time the main clock jitter as the total number of transitions (in particular for low magnitude input signals) is lower than the one generated by non-PWM ∆Σ modulators. At the same time, each DAC element carries the reference signal and the shaped quantization noise, resulting in a intrinsic DEM scheme which features low latency and high performances.

• The modulator has been simulated with MATLAB Simulink to assess the performances. Static and dynamic analog errors have been modeled and incorporated in each individual DAC element to confirm the previous statements. The feedback loop used is based on the Chebyshev type II filter to limit the out-of-band noise as it could potentially lead to instability. This has been carried out using the Delta-Sigma Toolbox by R. Schreier and the built-in “cheby2” MATLAB function.

Adopted methodologies

• The PWM modulation scheme is adopted to ensure that the transition density of each DAC element is kept constant whatever the input signal is. This has two effects: the ISI main contribution is translated to a mere DC offset and the signal is less affected by the main clock jitter as the total number of transitions (in particular for low magnitude input signals) is lower than the one generated by non-PWM ∆Σ modulators. At the same time, each DAC element carries the reference signal and the shaped quantization noise, resulting in an intrinsic DEM scheme which features low latency and high performances.

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Future work

• Another structure based on the previous premises is under study. It will allow even better performances (higher SNR and stability) but with a significant hardware overhead.

• These two novel topologies will be tested using an FPGA to verify the real life performances as the circuit is mostly digital thus easy to prototype.

• Thanks to the intrinsic low latency, low noise and high linearity, the modulators will be used in an ADC feedback loop to make the circuit “as most digital as possible”.

• As the overall frequency is low with respect to modern CMOS speeds, there is room for low power structures.

• The need of oversampling requires a good interpolation scheme. An interpolator based on the Discrete Cosine Transform (DCT) seems to be one of the best candidates. An efficient interpolation structure based on the DCT is under research.

List of attended classes

• 01QTEIU - Data mining concepts and algorithms (6/3/2018, 20 hours)

• 01S5URV - Intellectual Property Rights, Technology Transfer and Hi-Tech Entrepreneurship (22/3/2018, 30 hours)

• 01MNFIU - Parallel and distributed computing (27/6/2018, 25 hours)

• 01S5URV - Programmazione scientifica avanzata in matlab (20/4/2018, 20 hours)

• 01OSCIU - Reconfigurable computing (15/6/2018, 20 hours)

• 01SHCRV - Unsupervised neural networks (didattica di eccellenza) (9/4/2018, 30 hours)

• 01Q0RRV - Writing Scientific Papers in English (21/3/2018, 15 hours)